Roll No: | | | | | | | | | | | | |

BTECH
(SEM III) THEORY EXAMINATION 2025-26
DIGITAL SYSTEM DESIGN

TIME: 3 HRS   **M.MARKS: 70**

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1.   **Attempt all questions in brief.**   **02 x 7 = 14**

Q no.	Question	CO	Level
a.	Simplify the following expression using K-map: $f(A,B,C)=\sum m(0,1,2,3,4,5,6,7)$ K-मैप (कार्नो मानचित्र) का उपयोग करके निम्नलिखित व्यंजक को सरलीकृत कीजिए: $f(A, B, C) = \sum m(0, 1, 2, 3, 4, 5, 6, 7)$	1	K2
b.	Determine the value of base x, If $(193)_x = (623)_8$	1	K3
c.	Define cyclic codes.	2	K2
d.	What is race around condition?	3	K1
e.	Differentiate between Moore Machine and Mealey Machine.	3	K2
f.	What do you mean by noise margin?	4	K1
g.	Calculate the step size of a 10-bit ADC with 5 V reference.	5	K3

SECTION B

2.   **Attempt any three of the following:**   **07 x 3 = 21**

a.	Simplify the Boolean function. $F(w, x, y, z) = \sum m (1, 3, 7, 11, 15) + d (0, 2, 5)$. Also implement the minimized function using basic logic gates.	1	K3
b.	Describe a circuit of 4-bit binary adder-subtractor with overflow detection.	2	K2
c.	Design a 3-bit synchronous binary counter with neat sketch.	3	K2
d.	Explain the basic circuit and operation of emitter coupled logic (ECL).	4	K2
e.	Assume the following values for the ADC clock frequency = 1 MHz; V_T= 0.1 mV; DAC has F.S. output = 10.23 V and a 10-bit input. Determine the following values. i. The digital equivalent obtained for $V_A = 3.728$ V. ii. The conversion time. iii. The resolution of this converter. मान लीजिए निम्नलिखित मान दिए गए हैं: ADC क्लॉक फ्रीकेंसी = 1 MHz; V_T = 0.1 mV; DAC का F.S. आउटपुट = 10.23 V और 10-बिट इनपुट। निम्नलिखित मान ज्ञात कीजिए: i. V_A =3.728 V के लिए डिजिटल समकक्ष (Digital Equivalent) ii. रूपांतरण समय (Conversion Time) iii. इस कन्वर्टर का रिज़ॉल्यूशन (Resolution)	5	K2

SECTION C

3.   **Attempt any one part of the following:**   **07 x 1 = 07**

a.	Minimize the following using Quine-Mc Cluskey Method: $F (P, Q, R, S) = \sum m (0, 3, 5, 6, 7, 10, 12, 13) + d (2, 9, 15)$.	1	K2
b.	What do you mean by universal logic gates. Implement all other logic gates using universal logic gates.	1	K2
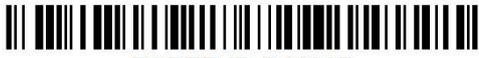
PAPER ID-311337

Roll No: | | | | | | | | | | | | |

BTECH
(SEM III) THEORY EXAMINATION 2025-26
DIGITAL SYSTEM DESIGN

TIME: 3 HRS

M.MARKS: 70

4.	**Attempt any *one* part of the following:**		07 x 1 = 07	
a.	What is magnitude comparator? Design a two-bit comparator circuit using logic gates.	2	K2
b.	Implement the following Boolean function using 4:1 MUX: $F(A, B, C, D) = \Sigma\, m\,(0, 1, 3, 4, 7, 8, 9, 11, 14, 15)$	2	K3

5.	**Attempt any *one* part of the following:**		07 x 1 = 07	
a.	Draw JK flip-flop and write the characteristic table and characteristic equation for it. Explain how will you convert it into T flip-flop.	3	K2
b.	With the help of neat sketch, explain the operation of 4-bit universal shift register.	3	K2

6.	**Attempt any *one* part of the following:**		07 x 1 = 07	
a.	Describe the construction of totem pole TTL NOR gate.	4	K2
b.	Design a 3-bit binary to Gray code converter using PLA.	4	K3

7.	**Attempt any *one* part of the following:**		07 x 1 = 07	
a.	An 8-bit ADC has a reference voltage of 5 V. (a) Calculate the resolution (b) Determine the quantization error (c) Find the digital output for an input of 2.6 V	5	K2
b.	What is the advantage of R/2R ladder DACs over those that use binary weighted resistors? A 10-bit DAC has a step size of 10 mV. Determine the full-scale output voltage and the percentage resolution. R/2R लैडर DAC के उन DACs पर क्या लाभ हैं जो बाइनरी ोटेड रेसिस्टर्स का उपयोग करते हैं? एक 10-बिट DAC का स्टेप साइज 10 mV है। फुल-स्केल आउटपुट ोल्टेज और प्रतिशत रिज़ॉल्यूशन ज्ञात कीजिए।		