PAPER ID-310596

Roll No: | | | | | | | | | | | | | |

BTECH
(SEM VII) THEORY EXAMINATION 2025-26
VLSI DESIGN

TIME: 3 HRS **M.MARKS: 70**

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1. Attempt *all* questions in brief. **02 x 7 = 14**

Q no.	Question	CO	Level
a.	Define sheet resistance.	1	K1
b.	Explain the propagation delay time in brief.	1	K2
c.	What is skin effect in interconnects?	2	K1
d.	What is the transient response of an interconnect?	2	K1
e.	List any two noise issues in dynamic CMOS design.	3	K1
f.	Interpret power consumption in CMOS circuits.	4	K2
g.	What is controllability in testability analysis?	5	K1

SECTION B

2. Attempt any *three* of the following: **07 x 3 = 21**

a.	Discuss the different design styles used in VLSI in brief. Explain any one style with its features and applications in detail.	1	K5
b.	Illustrate the concept of interconnection models in VLSI design and describe any two models briefly.	2	K4
c.	Explain the NORA CMOS (NP-Domino) logic circuit in detail, and provide a brief account of its advantages and disadvantages.	3	K5
d.	What do you mean by semiconductor memory? Explain its purpose in digital systems in detail.	4	K5
e.	Outline a concise note on (a) Linear Feedback Shift Registers and their use in testing. (b) Built-In Logic Block Observer and its functions.	5	K4

SECTION C

3. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Illustrate the VLSI design flow with the help of the Y-chart and provide a detailed explanation of each phase of the design methodology.	1	K4
b.	Construct the CMOS logic for the following Boolean expression (a) 3-input NAND gate (b) $Y = \overline{AB + (C + D).E}$	1	K6

4. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Provide a diagram of the lumped RC model for interconnects and illustrate its operation in detail.	2	K4
b.	Outline concise notes on the concepts of: (a) Logical effort (b) Parasitic delay	2	K4

5. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Design the following logic using domino CMOS logic $Y = AB + CD + EFG$ and compare it with the static CMOS design.	3	K6

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b.	Describe the working of static CMOS logic circuits. Also, compare static CMOS logic with dynamic CMOS logic.	3	K4

6. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain the operation of a three-transistor DRAM cell, incorporating the concepts of leakage currents and refresh operation.	4	K5
b.	Illustrate the circuit diagram of a 6T SRAM cell and describe its read and write operations in detail.	4	K4

7. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain Built-in Self-Test (BIST) techniques.	5	K5
b.	State the necessity of VLSI chip testing. Explain in detail the types of tests, including functional and manufacturing tests.	5	K5