Paper ID : 261466

Printed Page: 1 of 1

Subject Code:BEE401

Roll No:													

BTECH

(SEM. IV) THEORY EXAMINATION 2025-26

DIGITAL ELECTRONICS

TIME: 3 HRS **M.MARKS: 70**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2x7 = 14**

QNo.	Question	CO	Level
(a)	Convert the Octal number 245 into its decimal equivalent.	1	K3
(b)	Identify the logic gate that models a circuit with two switches connected in series.	1	K3
(c)	Explain the working of a multiplexer with an example.	2	K2
(d)	Illustrate the function of a flip-flop and give examples of any two types.	3	K2
(e)	For the design of a sequential circuit having nine states, Calculate the minimum number of memory elements required.	3	K3
(f)	Explain the basic function of an FPGA.	4	K2
(g)	Describe offset error in a D/A converter.	5	K2

SECTION B

2. Attempt any *three* of the following: **7 x 3 = 21**

(a)	Simplify the Boolean expression using K-map: F(A,B,C,D) = Σ(6,8, 10,11,15) +d(9,12,13,14). Implement using NAND gates only.	1	K3
(b)	Construct a full subtractor circuit and explain its operation.	2	K3
(c)	Explain the working of JK flip-flop with truth table. Also draw its State Diagram.	3	K3
(d)	Determine the most suitable logic family for a system requirement using given parameters such as power, speed, and noise immunity.	4	K3
(e)	A 4-bit R-2R ladder type D/A converter having resistor values of R=10kΩ and 2R=20kΩ, uses V_R of 10V. Calculate (a) the resolution of the D/A converter, and (b) I_0 for a digital input of 1101.	5	K3

SECTION C

3. Attempt any *one* part of the following: **7 x 1 = 7**

(a)	Analyze the given Boolean expressions and derive their canonical forms. 1. $AB + B\bar{C}D + \bar{A}D$ 2. $(A + \bar{B})(\bar{C} + \bar{D})(\bar{B} + \bar{C})$	1	K4
(b)	Examine the relationship between binary inputs and Gray code outputs in a 4-bit Binary to Gray Code converter.	1	K4

4. Attempt any *one* part of the following: **7 x 1 = 7**

(a)	Implement the logic function given below using a 74151 eight input data selector/MUX: Y(A,B,C,D)= Σ(2,4,6,7,9,10,11,12, 15)	2	K3
(b)	Apply the concept of cascading decoders to obtain outputs of a 5-to-32 decoder using two 4-to-16 decoders.	2	K3

5. Attempt any *one* part of the following: **7 x 1 = 7**

(a)	Examine the state diagram and excitation table of a synchronous decade counter implemented using Toggle flip-flops.	3	K4
(b)	Analyze the behavior of a finite state machine used for sequence detection and justify its state transitions.	3	K4

6. Attempt any *one* part of the following: **7 x 1 = 7**

(a)	Explain the construction and working of a TTL NAND gate with circuit diagram. Discuss its input-output characteristics.	4	K2
(b)	Describe the architecture and working of Programmable Logic Array (PLA).	4	K2

7. Attempt any *one* part of the following: **7 x 1 = 7**

(a)	Explain Flash Type ADC with relevant diagram. Discuss its applications.	5	K2
(b)	Interpret the operation of a 4-bit weighted resistor type D/A converter.	5	K2